AMENDMENTS TO THE CLAIMS

Please make the following amendments to the claims:

1. (Cancelled)

2. (Currently Amended)   ~~The system of claim 1~~ A system to derive symbol timing for a receiver, comprising:

a slicer configured to decode a received signal segment into a discrete data symbol;

a calculator configured to derive a symbol timing phase error based upon the received signal segment and discrete data symbol, and configured to compute an average based upon said symbol timing phase error, wherein the calculator comprises a multiplier and a leaky integrator ;

a circuit configured to receive the average and configured to develop a control signal based upon the average; and

an oscillator configured to receive the control signal and configured to generate symbol timing for a receiver.

3. (Cancelled)

4. (Currently Amended)   The system of claim [[1]] 2, wherein the circuit comprises a phase locked loop.

5. (Currently Amended)   The system of claim [[1]] 2, wherein the oscillator is a voltage controlled oscillator.

6. (Currently Amended)   The system of claim [[1]] 2, wherein the oscillator is configured to generate symbol timing for a transmitter.

7. (Currently Amended)   The system of claim [[1]] 2, wherein the system is part of a point-to-point system.

8-9. (Cancelled)

10. (Currently Amended)   The system of claim [[1]] 2, wherein the system is part of a multi-point system.

11-12. (Cancelled)

13. (Original) The system of claim 10, wherein the multi-point system operates on multiple virtual lines protocol.

14. (Cancelled)

15. (Currently Amended)   A system to derive symbol timing for a receiver, comprising The system of claim 14, further comprising :

a slicer configured to decode a received signal segment into a discrete data symbol;

a calculator configured to derive a symbol timing phase error based upon the received signal segment and discrete data symbol, and configured to compute an average based upon said symbol timing phase error;

a fractionally spaced forward equalizer configured to produce a plurality of coefficients;

a centroid error calculator configured to produce a centroid error based on the plurality of coefficients received from the fractionally spaced forward equalizer ;

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a circuit configured to receive the average and configured to develop a control signal based upon the average; and

an oscillator configured to receive the control signal and configured to generate symbol timing for a receiver.

16. (Previously Presented)   The system of claim 15, wherein the calculator is configured to subtract the centroid error from the average.

17. (Currently Amended)   A system to derive symbol timing for a receiver ~~The system of claim 13, further~~ comprising:

a slicer configured to decode a received signal segment into a discrete data symbol;

a calculator configured to derive a symbol timing phase error based upon the received signal segment and discrete data symbol, and configured to compute an average based upon said symbol timing phase error;

a circuit configured to receive the average and configured to develop a control signal based upon the average;

an oscillator configured to receive the control signal and configured to generate symbol timing for a receiver; and

a dual eye close structure, the first eye close being coupled to the received signal segment and the second eye close being coupled to an output of a decision feedback equalizer, wherein the dual eye close structure is configured to control a switch to remove the signal path from the calculator to the circuit.

18. (Previously Presented)   A system to track symbol timing for a receiver, comprising:

a forward equalizer configured to receive a signal segment and configured to produce an equalized signal based upon a plurality of coefficients applied to the received signal segment;

a centroid error calculator configured to receive a plurality of coefficients from the forward equalizer and configured to calculate a centroid error from the plurality of coefficients and a nominal number based upon the plurality of coefficients;

a first subtractor configured to receive the equalized signal from the forward equalizer and a noise correction calculated by a decision feedback equalizer, and configured to calculate a first difference based upon the equalized signal and the noise correction;

a first phase rotator configured to receive the first difference from the first subtractor and an inverted result of a phase corrector, and configured to produce a square signal based upon the first difference and the inverted result;

a slicer configured to receive the square signal from the first phase rotator, and configured to decode the square signal into a discrete data symbol;

a first multiplier configured to receive the first difference and the discrete data symbol, and configured to derive a timing phase error therefrom;

a leaky integrator configured to receive the timing phase error and the centroid error calculation and configured to produce an average timing phase error based upon the timing phase error and the centroid error calculation;

a switch configured to receive the average timing phase error and an eye close signal from a first and second eye close function, and further configured to open a connection to a phase locked loop when the eye close signal is asserted, the eye close signal being asserted by the first or second eye close functions when no received signal segment is sensed;

a phase locked loop configured to receive the average timing phase error when the switch

is closed and configured to produce a control voltage; and

a voltage controlled oscillator configured to receive the control voltage from the phase

locked loop and further configured to generate symbol timing for a receiver.

19. (Currently Amended)   A system to track symbol timing for a receiver, comprising:

means for decoding a received signal segment into a discrete data symbol;

means for calculating a symbol timing phase error, based upon the received signal

segment and discrete data symbol, and an average symbol timing phase error;

means for creating a control signal based upon the average symbol timing phase error;

and

means for equalizing the received signal;

means for computing a centroid error based upon coefficients of the equalizing means;

means for subtracting the centroid error from the average symbol timing phase error; and

means for receiving the control signal and generating symbol timing for a receiver.

20-22. (Cancelled)

23. (Currently Amended)   A method for deriving symbol timing The method of claim

21, further comprising the steps of:

decoding a received signal segment into an discrete data symbol;

equalizing the received signal with a forward equalizer;

calculating a symbol timing phase error and an average symbol timing phase error based

upon the received signal segment and discrete data symbol;

calculating the centroid of the coefficients of the forward equalizer; and

subtracting the centroid of the coefficients of the forward equalizer from the average ;

creating a control signal based upon the average symbol timing phase error; and

generating symbol timing for a receiver based upon the control signal.

24. (Currently Amended)   A method for deriving symbol timing The method of claim

21, further comprising the steps of:

decoding a received signal segment into an discrete data symbol;

calculating a symbol timing phase error and an average symbol timing phase error based

upon the received signal segment and discrete data symbol;

creating a control signal based upon the average symbol timing phase error;

generating symbol timing for a receiver based upon the control signal; using a first eye

close test on the received signal;

cleaning noise from the received signal with a decision feedback equalizer;

using a phase corrector to put a constellation in a correct orientation;

using a second eye close test on the constellation; and

opening a flywheel switch when an output of the first or second eye close is asserted.

25. (Currently Amended)   A system to derive symbol timing for a receiver,

comprising:

an equalizer configured to receive an incoming signal and to produce an equalized signal,

the equalizer having a plurality of coefficients;

a means for updating the plurality of coefficients of the equalizer based on the reference

signal and the equalized signal;

a slicer configured to decode the equalized signal into a reference signal; and

a means for comparing the reference signal and the equalized signal and configured to produce a symbol timing phase error;

an averager configured to produce an average symbol timing phase error based upon the symbol timing phase error;

a control circuit configured to receive the average symbol timing phase error and configured to develop a control signal based upon the average symbol timing phase error;

an oscillator that receives the control signal and that generates the symbol timing signal; and

a dual eye close structure, the first eye close being coupled to the equalized signal and the second eye close being coupled to an output of a decision feedback equalizer, wherein the dual eye close structure is configured to remove the signal path between the averager and the control circuit.

~~a symbol timing calculator configured to derive a symbol timing signal based upon the equalized signal and the reference signal.~~

26. (Cancelled)

27. (Previously Presented)   The system of claim 25, wherein the equalizer comprises a fractionally spaced forward equalizer.

28-31. (Cancelled)

32. (Currently Amended)   A system to derive symbol timing for a receiver ~~The system of claim 25, further~~ comprising:

an equalizer configured to receive an incoming signal and to produce an equalized signal, the equalizer having a plurality of coefficients;

a slicer configured to decode the equalized signal into a reference signal;

a symbol timing calculator configured to derive a symbol timing signal based upon the equalized signal and the reference signal; and

a centroid error calculator configured to produce a centroid error based on the plurality of coefficients received from the equalizer, wherein the symbol timing calculator is further configured to derive a symbol timing signal based upon the equalized signal, the reference signal, and the centroid error.

33. (Previously Presented) The system of claim 25, further comprising:

a decision feedback equalizer configured to receive the reference signal and to produce a DFE-compensated signal; and

a subtractor configured to subtract the DFE-compensated signal from the equalized signal, wherein the resulting signal is input into the slicer.

34. (New) A system to derive symbol timing for a receiver, comprising:

an equalizer configured to receive an incoming signal and to produce an equalized signal, the equalizer having a plurality of coefficients;

a centroid error calculator configured to produce a centroid error based on the plurality of coefficients received from the equalizer;

a slicer configured to decode the equalized signal into a reference signal; and

a symbol timing calculator configured to derive a symbol timing signal based upon the equalized signal and the reference signal and to derive a symbol timing signal based upon the equalized signal, the reference signal, and the centroid error.